UNITED STATES PATENT APPLICATION

HIGH PERFORMANCE, LOW COST MICROELECTRONIC CIRCUIT PACKAGE WITH INTERPOSER

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Client Ref. No. P10665

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FIELD OF THE INVENTION

The invention relates generally to microelectronic circuits and, more particularly, to structures and techniques for packaging such circuits.

BACKGROUND OF THE INVENTION

After a microelectronic circuit chip (i.e., a die) has been manufactured, the chip is typically packaged before it is sold to the public. The package provides both protection for the chip and a convenient and often standardized method for mounting the chip within an external system. The circuit package must include some means for providing electrical communication between the various terminals of the circuit chip and the exterior environment. Many different packaging technologies have been used in the past for providing this communication. The type of package that is used for a particular chip can have a significant impact on the performance of the completed device. Typically, in a high volume manufacturing environment, cost will be a primary concern in selecting a packaging technology. Performance is also a very important criterion. As circuits get smaller and faster, there is an ongoing need for innovative and cost effective packaging technologies.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified cross sectional side view of a microelectronic device in accordance with one embodiment of the present invention;

Fig. 2 is a simplified cross sectional side view of a microelectronic device in accordance with another embodiment of the present invention;

Fig. 3 is a cross-sectional isometric view of the die/core assembly of Fig. 1 before a build up metallization layer is deposited;

Fig. 4 is a cross-sectional isometric view of the die/core assembly of Fig. 3 after a dielectric layer has been deposited;

Fig. 5 is a schematic top view of a microelectronic die having a plurality of conductive contacts in accordance with one embodiment of the present invention;

Fig. 6 is a schematic top view of a metallization pattern for a build up metallization layer in accordance with one embodiment of the present invention;

Fig. 7 is an enlarged schematic view of a central portion of the metallization pattern of Fig. 6 illustrating an arrangement of power and ground pads therein;

Fig. 8 is a schematic top view illustrating a portion of a metallization pattern in accordance with another embodiment of the present invention; and

Fig. 9 is a schematic top view illustrating a portion of a metallization pattern in accordance with yet another embodiment of the present invention.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein in connection with one embodiment may be implemented within other embodiments without departing from the spirit and scope of the invention. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views.

The present invention relates to low cost structures and techniques for packaging microelectronic circuit chips. A die is fixed within an opening in a package core to form a die/core assembly. At least one metallic build up layer is then formed on the die/core assembly and a grid array interposer unit is laminated to the assembly. The grid array interposer unit includes an array of contacts that allow it to be mounted to an external circuit board using a corresponding mounting technique (e.g., ball grid array (BGA), land grid array (LGA), pin grid array (PGA), surface mount technology (SMT), and/or others). In one embodiment of the invention, one or more capacitors is mounted to a surface of the grid array interposer unit on a side opposite the die/core assembly to provide a de-coupling capacitance having relatively low series inductance for the circuitry of the die. In another embodiment, one or more capacitors are mounted directly to a metallization layer on the die/core assembly to provide a de-coupling capacitance having even lower series inductance. The techniques and structures of the present invention are capable of supporting high performance circuit operation and can thus be used to package high performance products, such as desktop and server segments. In addition, the inventive techniques and structures can provide this high performance operation at a relatively low cost compared to other high performance packaging schemes.

Fig. 1 is a simplified cross sectional side view of a microelectronic device 10 in accordance with one embodiment of the present invention. As illustrated, the device 10 includes: a microelectronic die 12, a package core 14, a build up metallization layer 16, a grid array interposer unit 18, and at least one de-coupling capacitor 20. The die 12 is fixed within an opening 24 in the package core 14 using an encapsulation material 22. As will be described in greater detail, the metallization layer 16 is built up upon the die/core assembly to provide escape routing and pitch expansion for contact structures on the die 12. In at least one embodiment, only a single build up metallization layer 16 is used (although multi-layer embodiments also exist). The grid array interposer unit 18 provides for electrical communication between the die/core assembly described above and an external circuit board (e.g., a computer motherboard). The grid array

interposer unit 18 is laminated to the die/core assembly using any of a variety of different lamination techniques. The grid array interposer unit 18 has a metallization pattern on a first surface 26 thereof that is conductively coupled to the build up metallization layer 16 of the die/core assembly during the lamination process. The grid array interposer 18 also includes an array of conductive contacts on a second surface 28 thereof for subsequent connection to the external circuit board. The grid array interposer 18 can also include various intermediate metal layers between the first and second surfaces 26, 28 to perform, for example, additional routing functions or to provide a ground and/or power plane within the device 10. In one embodiment, the grid array interposer 18 is a relatively inexpensive (e.g., below $1 per unit), coarse pitch structure. In addition, the grid array interposer 18 will preferably be a relatively low profile structure (e.g., < 0.5 millimeters(mm)) to allow reduced through hole pitch and minimal inductance for the de-coupling capacitors.

The metallization pattern on the first surface 26 of the grid array interposer 18 includes conductive portions that correspond to portions (e.g., landing pads) on the metallization layer 16 of the die/core assembly. During lamination, this metallization pattern is conductively coupled to the metallization layer 16 so that corresponding conductive elements are connected together. In one lamination technique, a solder mask is first patterned on the first surface 26 of the interposer 18 to define lands on the unit. Solder or conductive epoxy is then applied to the exposed land surfaces using a known technique (e.g., screen printing). The interposer 18 is then directly laminated to the metallization layer 16 in a known manner (e.g., solder reflow, ultrasonic bonding, etc.). In another technique, an anisotropically conductive film is used to attach the two structures. Some well known lamination processes that can be used include standard hydraulic lamination, vacuum assisted hydraulic lamination, autoclave, and mass lamination. As will be apparent to persons of ordinary skill in the art, other lamination techniques can also be used.

In one embodiment, a relatively simple two layer interposer unit 18 is used. The only routing within this interposer structure is from the landing pads on the first surface

26 of the unit to corresponding plated through holes and from the plated through holes to corresponding conductive contacts on the second surface 28. As will be appreciated, greater routing flexibility can be achieved by increasing the number of layers within the interposer 18.

As illustrated in Fig. 1, the de-coupling capacitors 20 are connected to the second surface 28 of the grid array interposer 18 in a region below the die 12. Because of the low profile of the package, capacitive de-coupling can be provided in this manner with relatively low series inductance. To achieve even less series inductance, the de-coupling arrangement of Fig. 2 can be implemented. In this embodiment, an opening 34 is provided in the interposer 18 that allows the de-coupling capacitors 20 to be mounted directly to the metallization layer 16 on the die/core assembly. Thus, the capacitors 20 can be mounted extremely close to the die 12 (e.g., less than 100 micrometers in one implementation) with the series inductance being correspondingly low. As will be described in greater detail, in at least one embodiment, a special landing pad configuration is provided within the metallization layer 16 to facilitate connection of the de-coupling capacitor(s) 20 to the metallization layer 16 below the die 12. It should be appreciated that the present invention does not require the connection of de-coupling capacitors to either the interposer 18 or the metallization layer 16. For example, in one embodiment of the invention, de-coupling capacitors are provided on the underside of the circuit board onto which the microelectronic device is mounted. Other de-coupling arrangements can also be used.

Any of a variety of techniques can be used to mount the microelectronic device 10 to an external circuit board. These techniques can include, for example, land grid array (LGA), ball grid array (BGA), or pin grid array (PGA) techniques. In the illustrated embodiment, an array of pins 30 is provided on the second surface 28 of the interposer 18 to provide connection to the external circuit board. In a preferred approach, the pins 30 are attached to the interposer 18 before the interposer 18 is laminated to the die/core assembly. In this manner, yield loss during the pin attach process does not result in the loss of known good die.

Fig. 3 is a cross-sectional isometric view of the die/core assembly of Fig. 1 before a build up metallization layer is deposited. To facilitate understanding of the build up process, the die/core assembly of Fig. 3 is inverted with respect to the structure of Fig. 1. As shown, the microelectronic die 12 is fixed within an opening 24 in the package core 14 using an encapsulation material 22. The microelectronic die 12 includes electronic circuitry that is implemented on one or more internal layers. Although not shown in Fig. 3, a plurality of conductive contacts are distributed on the upper surface of the die 12 to provide an electrical interface to the circuitry of the die 12. The package core 14 can be formed from any of a variety of materials including, for example, bismaleimide triazine (BT), resin-based materials, flame retarding glass/epoxy materials (e.g., FR4), polyimide materials, ceramic materials, metal materials (e.g., copper), and others. A metal core material has the advantage that it will also serve as a heat spreader to facilitate heat removal from the die 12. In the illustrated embodiment, the package core 14 is formed from a dielectric board material (e.g., a BT board) having a conductive cladding 20 (e.g., copper foil) covering at least one surface thereof. In one embodiment, for example, a 0.725mm thick board material having part number CCL-HL830 and manufactured by Mitsubishi Gas and Chemical Company is used to form the package core. As will be described in greater detail, the conductive cladding 20 can be used as a ground plane within the microelectronic device 10 to provide impedance control for transmission structures therein.

The opening 24 within the package core 14 can extend through the core 14 (as illustrated in Fig. 3) or a floor portion can be provided within the opening 24 to support the die 12 during packaging. The encapsulation material 22 can include any of a variety of materials that are capable of holding the die 12 within the core 14 including, for example, various plastics, resins, epoxies, elastomers, and the like. Preferably, the encapsulation material 22 will be non-conductive. In the illustrated embodiment, the upper surface of the die 12, the upper surface of the encapsulation material 22, and the upper surface of the core 14 are made substantially flush with one another. In another embodiment, the upper surface of the die 12 is higher than that of the core 14 and the

encapsulation material 22 forms a layer above the core 14 that is flush with the upper surface of the die 12. Other arrangements for mounting the die 12 within the package core 14 can also be used.

After the die 12 has been fixed within the core 14, a layer of dielectric material 32 is deposited on the upper surface of the die/core assembly, as shown in Fig. 4. Any of a variety of different materials can be used for the dielectric layer 32 including, for example, glass particle filled epoxy resins (e.g., Ajinomoto Buildup Film (ABF) available from Ajinomoto), bisbenzocyclobutene (BCB) (available from Dow), polyimide, silicone rubber materials (e.g., DC6812 from DowCorning), various low-k dielectrics (e.g., SiLK from Dow Chemical), IPN (available from Ibiden), and others. A plurality of via holes (not shown) are formed through the dielectric layer 32 to expose portions of the contacts on the die 12. As will be described in greater detail, a metallization layer is then formed on the upper surface of the dielectric layer 32. The metallization layer includes a plurality of metallic elements that are each conductively coupled to corresponding contacts on the die 12 through one or more of the via holes. Additional layers (i.e., dielectric and metal) may then be built up over the first metallization layer in a similar manner. The uppermost metallization layer will include a metallization pattern that corresponds to the pattern on the first surface 26 of the interposer 18. As described above, in at least one embodiment, only a single metallization layer is built up upon the die/core assembly. This single metallization layer can be built up on panels mounted back to back, thus halving the build up cost. As will be appreciated, the use of a single metallization layer can reduce manufacturing costs significantly.

Fig. 5 is a top view of a microelectronic die 12 in accordance with one embodiment of the present invention. As shown, the die 12 includes a plurality of conductive contacts distributed on an upper surface thereof. That is, the die 12 includes a number of signal pads 36 within a peripheral region of its upper surface and a number

of power and ground bars 38, 40 within a central region thereof. The signal pads 36 act as signal input/output (I/O) terminals for the circuitry of the die 12 (e.g., to transfer data or clock signals). In one approach, the signal pads 36 include short, wide copper bumps that cover the signal bond pad openings of the die 12 (using, for example, an alternative bump metallurgy (ABM) controlled collapse chip connection (C4) process). Other arrangements can also be used (e.g., the signal bond pad openings through the die passivation layer can be left uncovered). In the illustrated embodiment, a single row of signal pads 36 is provided on each side of the die 12. Other configurations, including multiple row configurations and random (non-aligned) configurations, can also be used.

The power and ground bars 38, 40 are arranged in an alternating pattern on the active surface of the die 12. In one approach, each of the power and ground bars 38, 40 includes a copper bar that links the power or ground bond pads of the die 12 in a particular row. Such bars can be formed, for example, as part of the C4 metallization. Each of the power bars 38 is coupled to circuit nodes within the die 12 that require application of a predetermined supply potential (e.g., V_{DD}) during circuit operation. Similarly, each of the ground bars 40 is coupled to circuit nodes within the die 12 that require a different supply potential (e.g., V_{SS}) during circuit operation. The number of signal pads 36, power bars 38, and ground bars 40 on the die 12 will typically depend upon the complexity and arrangement of the circuitry within the die 12. It should be appreciated that many alternative contact patterns can be used for the die 12 in accordance with the present invention and the particular pattern illustrated in Fig. 5 is not meant to be limiting.

Fig. 6 is a top view of a metallization pattern 44 that is deposited on the dielectric layer 32 of the die/core assembly (see Fig. 4) in accordance with one embodiment of the present invention. This metallization pattern 44 forms a single metallization layer that is build up upon the die/core assembly to allow for direct connection (lamination) to the interposer 18. In Fig. 6, the outlines of the underlying die 12 and the opening 24 in the package core 14 are shown using hidden lines. As

illustrated, the metallization pattern 44 includes a plurality of I/O landing pads 46 within a peripheral region thereof (i.e., above the package core) for use in coupling I/O signals to and from the interposer 18. The metallization pattern 44 also includes power landing pads 52, 54 and ground landing pads 56, 58 within a central region thereof (i.e., above the die 12) for use is making power and ground connections to the interposer 18. Both the I/O landing pads 46 and the power and ground landing pads 52, 54, 56, 58 have a pitch that is consistent with corresponding structures on the first surface 26 of the interposer 18. In the illustrated embodiment, the metallization pattern 44 includes two power landing pads and two ground landing pads. In general, it is desirable to use as many power and ground landing pads as is consistent with the pitch limitation of the device to minimize inductance. In the illustrated embodiment, the I/O landing pads 46 and the power and ground landing pads 52, 54, 56, 58 are square in shape. It should be appreciated, however, that any of a wide variety of shapes can be used including, for example, rectangular and circular shapes.

Each of the I/O landing pads 46 is conductively coupled to a corresponding signal pad 36 on the active surface of the die 12 (see Fig. 5) through a path including a transmission segment 48. The transmission segments 48 thus provide the "escape routing" for the signal connections of the die 12. Each transmission segment 48 is connected at a distal end to a terminal pad 50 within the metallization pattern 44 that is conductively coupled to the associated signal pad 36 on the die 12 through one or more via connections (e.g., microvias). The number of I/O signal connections that can be made within a particular microelectronic device will typically depend upon the density of transmission segments 48 that can be reliably implemented on the build up metallization layer. In at least one embodiment of the invention, multiple rows of I/O landing pads 46 are implemented within the build up metallization layer.

Fig. 7 is an enlarged view of the metallization pattern 44 of Fig. 6 in the vicinity of the power landing pads 52, 54 and the ground landing pads 56, 58. In Fig. 7, the power and ground bars 38, 40 on the underlying die 12 are shown using hidden lines. As illustrated, the power landing pads 52, 54 are each conductively coupled to multiple

power bars 38 on the underlying die 12 using a plurality of via connections 60 that extend through the dielectric layer 32. Similarly, the ground landing pads 56, 58 are each conductively coupled to multiple ground bars 40 on the underlying die 12 using via connections 60. The number of power and ground bars 38, 40 that are encompassed by a power landing pad 52, 54 or a ground landing pad 56, 58 will normally depend upon the increase in pitch that is desired and the amount of series inductance that can be tolerated. The number of via connections 60 that are used in a particular implementation to couple a power or ground bar to a power or ground landing pad will usually depend upon the level of series resistance that can be tolerated and/or the maximum allowable current in the supply path.

Referring back to Fig. 6, the metallization pattern 44 may also include a ground pad 42 that is conductively coupled to the conductive cladding 20 of the underlying package core 14 through one or more via connections (or similar structures) in the dielectric layer 32. During package assembly, this ground pad 42 is conductively coupled to a corresponding ground structure on the interposer 18 that will be tied to ground when the microelectronic device 10 is mounted within an external circuit. The ground pad 42 can also be directly coupled to the ground of the die 12 by a trace portion (not shown) within the metallization pattern 44 that is connected to one or more ground bars 40 on the die 12 through via connections. In this manner, the conductive cladding 20 will be grounded during subsequent operation of the microelectronic device 10 and will serve as a ground plane beneath the metallization pattern 44. This ground plane allows transmission lines having a controlled impedance (e.g., microstrip lines) to be provided on the build up metallization layer (i.e., to form the transmission segments 48). In at least one embodiment, a second ground plane is provided on an intermediate layer of the interposer unit 18 that allows stripline transmission lines to be formed on the build up metallization layer. Among other advantages, controlled impedance lines are usually capable of significantly higher operational speeds than lines having a non-controlled impedance. Space providing, any number of ground pads 42 can be implemented as part of the build up metallization layer.

In an alternative approach, the conductive cladding 20 of the package core 14 is used as a power plane. In this approach, the pad 42 is coupled to a power source through the interposer 18 rather than ground. The power plane will still operate as a signal return structure for the transmission lines of the build up metallization layer.

After the metallization pattern 44 has been deposited, a solder mask can be applied over the pattern 44 to mask areas that will not be connected to the interposer 18. The exposed areas can then be processed in accordance with the lamination method that will be used to attach the die/core assembly to the interposer 18. In an alternative approach, the solder mask could be patterned across the active surface and simultaneously act as an adhesive for attachment of the interposer. As described above, any of a number of different methods can be used to laminate the die/core to the interposer 18. Preferably, a lamination technique will be used that will accommodate any dimensional changes that might occur due to differences in the coefficient of thermal expansion between the various materials.

As described previously, the power and ground landing pads 52, 54, 56, 58 illustrated in Figs. 6 and 7 will be conductively coupled to corresponding structures on the first surface 26 of the interposer 18 during package assembly. As can be appreciated, this will leave little or no room for attachment of de-coupling capacitors to the build up metallization layer in the region above the die 12. Thus, the metallization pattern 44 of Figs. 6 and 7 is more appropriate for use in systems that do not attach the de-coupling capacitors directly to the die/core assembly (e.g., systems where the de-coupling capacitors are mounted to the second surface 28 of the interposer 18). Fig. 8 illustrates a portion of a metallization pattern 64 that allows direct mounting of the de-coupling capacitors to the metallization layer 16 of the die/core assembly. To simplify illustration and facilitate understanding, the outer portion of the metallization pattern 64 (i.e., the I/O portion) is not shown in Fig. 8. The outer portion, however, will typically be similar to that of the metallization pattern 44 of Fig. 6. The border of the underlying die 12 is shown in Fig. 8 using hidden lines. The power and ground bars 38, 40 on the underlying die 12 are also shown using hidden lines (the die 12 includes eight

power bars 38 and eight ground bars 40). The opening 34 in the interposer unit 18 (see Fig. 2) is projected onto the metallization pattern 64 of Fig. 8 using a dotted line.

As illustrated in Fig. 8, the metallization pattern 64 includes a plurality of power landing pads 70, 72, 74, 76, 78, 80, 82, 84, 86, 88 and a plurality of ground landing pads 90, 92, 94, 96, 98, 100, 102, 104, 106, 108. As before, the power landing pads 70, 72, 74, 76, 78, 80, 82, 84, 86, 88 are each conductively coupled to multiple power bars 38 on the underlying die 12 using via connections 110 and the ground landing pads 90, 92, 94, 96, 98, 100, 102, 104, 106, 108 are each conductively coupled to multiple ground bars 40 on the underlying die 12 using via connections 110. The power and ground landing pads outside the boundary of the opening 34 (i.e., power landing pads 70, 78, 80, 88 and ground landing pads 94, 96, 104, 106) are used to make power and ground connections to the interposer 18, as described previously. The power and ground landing pads inside the boundary of the opening 34 (i.e., power landing pads 72, 74, 76, 82, 84, 86 and ground landing pads 90, 92, 98, 100, 102, 108) are used to connect de-coupling capacitors to the build up metallization layer. The de-coupling capacitors will preferably be mounted over the part of the die with the greatest demand for rapid delivery of power (e.g., the fireball). In one approach, one or more de-coupling capacitors are connected between each adjacent pair of power and ground landing pads within the opening 34. In another approach, an array capacitor is connected to multiple pads. As will be appreciated, other capacitor mounting configurations are also possible.

In the embodiment of Fig. 8, the opening 34 in the interposer 18 is smaller than the upper surface of the die 12. As the opening 34 in the interposer unit 18 gets larger, as would occur when more coupling capacitors are required, there is less space for power and ground landing pads above the die 12 for connection to the interposer 18. Fig. 9 illustrates a portion of a metallization pattern 112 that can be used when the opening 34 in the interposer 18 is too large to allow power and ground landing pads to be implemented above the die 12 for connection to the interposer 18. As shown, the metallization pattern 112 includes a plurality of power landing pads 114, 116, 118, 120,

122, 124, 126, 128 and a plurality of ground landing pads 130, 132, 134, 136, 138, 140, 142, 144 in a region above the die 12 and within the boundary of the opening 34. As before, these power and ground landing pads are used for connection of the de-coupling capacitors.

In addition, the metallization pattern 112 includes first and second traces 146, 148 that are used to conductively couple the power and ground bars 38, 40 on the die 12 to power and ground landing pads 150, 152, 154, 156 that are beyond the outer boundaries of the die 12 and the opening 34. In general, a plurality of such traces may be implemented in order to meet electrical requirements of the package, such as maximum current and loop inductance. The first trace 146 is connected to each of the power bars 38 on the underlying die 12 using via connections 160 and also to power landing pads 150 and 152. Similarly, the second trace 148 is connected to each of the ground bars 40 on the underlying die 12 using via connections 160 and also to ground landing pads 154 and 156. The power landing pads 150, 152 and the ground landing pads 154, 156 are to be conductively coupled to corresponding structures on the interposer 18 during the lamination process.

It should be appreciated that many alternative metallization patterns can be used for the build up metallization layer 16 of the die/core assembly in accordance with the present invention and the particular patterns illustrated in Figs. 6, 7, 8, and 9 are not meant to be limiting. In addition, as described previously, microelectronic devices using multiple build up metallization layers on the die/core assembly can also be implemented. For example, a second build up layer can be used to increase the area available in the center region for de-coupling capacitors. Alternatively, a second build up layer can be used to provide additional ground structures for the transmission segments 48 (e.g., an upper ground plane for a strip line configuration). Also, a second build up layer can be used to provide additional flexibility in routing the I/O and power/ground traces. Other multiple layer configurations also exist.

Although the present invention has been described in conjunction with certain embodiments, it is to be understood that modifications and variations may be resorted

to without departing from the spirit and scope of the invention as those skilled in the art readily understand. Such modifications and variations are considered to be within the purview and scope of the invention and the appended claims.

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